Notice of References Cited	Application/Control No. 10/605,308	Applicant(s)/Patent Under Reexamination CHEN ET AL.	
	Examiner Anh D. Mai	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-4,906,589	03-1990	Chao, Fung-Ching	438/305
	B	US-4,907,048	03-1990	Huang, Tiao-Yuan	257/344
	C	US-5,146,291	09-1992	Watabe et al.	257/344
	D	US-5,175,119	12-1992	Matsutani, Takeshi	438/290
	E	US-5,241,203	08-1993	Hsu et al.	257/344
	F	US-5,256,585	10-1993	Bae, Dong-Joo	438/304
	G	US-5,276,347 A	01-1994	Wei et al.	257/388
	H	US-5,521,115 A	05-1996	Park et al.	438/243
	I	US-5,643,833	07-1997	Tsukamoto, Masanori	438/636
	J	US-6,274,441 B1	08-2001	Mandelman et al.	438/286
	K	US-6,426,247 B1	07-2002	Divakaruni et al.	438/185
	L	US-2001/0038113	11-2001	Bronner et al.	257/301
	M	US-2002/0055224	05-2002	Mandelman et al.	438/243

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP-2004-146839	05-2004	Japan	Yamazaki et al.	H01L 21/336
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	D.S. Wen et al., A Self-Aligned Inverse-T Gate Fully Overlappsed LDD for Sub-Half Micron CMOS. IEDM 1989, pp. 765-768
	V	J.R. Pfiester et al., A Self-Aligned LDD/Channel Implanted ITLDD Process with Selectively-Deposited Poly Gates for CMOS VLSI. IEDM 1989, pp. 769-772.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.